A Novel Vector-Locked Loop Scheme for Synchronized Extraction of Harmonics

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***Abstract*—The separation of the fundamental from a distorted waveform is an important component in the implementation of a custom power device. A novel scheme for a vector-locked loop (VLL) for synchronous extraction of harmonics/fundamental in a distorted periodic waveform is described here. An intuitive, though approximate, explanation is provided for the operation of the algorithm, focusing on the locking process and the filtering capability. Performance aspects are analysed and an approximate linear time-invariant model is presented to facilitate in the design. Moreover, a means for choosing design parameters to achieve the optimum performance is provided. Main features of the proposed VLL are its simplicity, excellent insensitivity to harmonics, noise rejection, availability of both fundamental and harmonics without additional processing, and the speed of operation. The claims are verified through extensive simulation studies in MATLAB®/Simulink®.**

***Keywords*—Vector-locked loop, amplitude-locking, phase-locking, harmonics extraction, amplitude demodulation**

I. Nomenclature

$x_I(t)$	Instantaneous value of input signal.
$C_k(t)$	Instantaneous amplitude of k^{th} harmonic in x_I.
ω_o	Frequency of fundamental component in x_I.
ϕ_k	Phase shift ($\phi_k>0 \Rightarrow$ lead) of k^{th} harmonic in x_I.
$x_O(t)$	Instantaneous value of output signal.
$a_O(t)$	Instantaneous amplitude of x_O.
$A_O(t)$	dc component in a_O.
$x_E(t)$	Instantaneous value of error signal.
$X_E(t)$	dc component in x_E.
B_P	Amplitude of phase-locked loop (PLL) output.
ω_n	Natural frequency of the second-order low-pass filter.
Q	Quality factor of the second-order low-pass filter.
G	Integrator gain.

II. Introduction

The extraction of harmonics or the fundamental components of voltages and/or currents is one of the main parts in the implementation of custom power devices.The techniques available can be broadly classified into single-phase and three-phase. They can also be classified into open-loop techniques and closed-loop techniques. A comparative evaluation of some of these methods may be found in [1] and the importance and applications of proper extraction may be found in [2]. The closed-loop techniques have the distinct advantage of being able to stay synchronised (zero-deviation, amplitude/phase-locked, to be more precise) to the input, which is very important in all applications connected to the grid. Extracting the fundamental/harmonics in a single-phase signal in a closed-loop scheme is the main focus of this paper. The proposed scheme falls into the class of closed-loop techniques presented in [3]–[7].

Amplitude locking has been in use in the communication area for the purpose of amplitude modulation/demodulation. A vector-locked loop was presented in a patent by DaSilva [6] which uses peak-detection in the magnitude detection stage. An amplitude-locked loop was presented in another patent by Pettigrew [8]. Both the aforementioned schemes assume the input to be a sinusoid and hence can not be used for distorted waveforms.

In the area of synchronised filtering the scheme presented in 1995 by Luo, et. al., [4] has the desirable feature of staying locked to the PLL reference and is very simple to understand and implement. However its settling time is a function of the integrator gain but an increase in the gain, to improve dynamic performance, results in increased distortion in the filtered output. In [3] Moir has presented an analysis of the amplitude servo by Pettigrew [8] for the purpose of amplitude demodulation. This has features similar to those of the scheme mentioned above. A vector-locked loop for synchronous extraction of harmonics was presented for the first time in 2002 by M. Karimi-Ghartemani, et al. [5]. The performance is similar to that of the scheme presented by Luo, et al., since it uses the same structure in the amplitude extraction section of the algorithm. An improved scheme was presented by H. Karimi et al., in [7] in 2003, where a low-pass filter is introduced in cascade with the integrator which improves the steady-state response and also allows for a higher gain in-turn reducing the settling-time.

In this paper a novel scheme (also based on a locked loop) for extraction of harmonics is presented. Its unique feature is the use of a second-order low-pass filter (SOLF) pre-tuned to a center frequency (ω_n) for extracting the residual fundamental and dc components to drive the integrator to the

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amplitude of the fundamental. Thus it renders the steady-state and transient performances superior to the techniques known so far. Moreover design considerations while choosing G and Q optimally to achieve a better performance are discussed here. In addition to being used for harmonic extraction it can also be used for amplitude/frequency demodulation in communication systems.

The paper is organised as follows: In Section III, the operation of the proposed scheme is explained. The approximate transient analysis and linear time invariant (LTI) model development is presented. Section IV deals with the steady-state analysis including performance for tracking and distortion. In Section V, the stability analysis is presented and the effects of G and Q on the steady-state and transient performances are discussed. Design considerations are dealt with in Section VI and simulation results are presented in Section VII.

III. The Proposed VLL

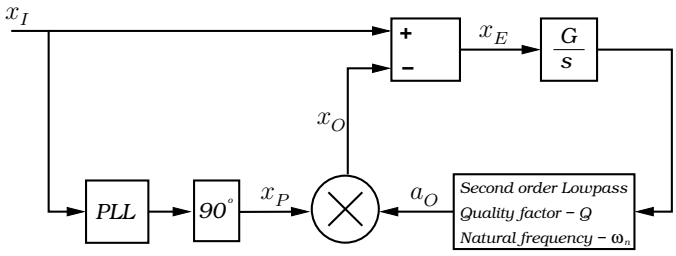

Fig. 1. Block diagram of proposed VLL

The proposed VLL (Fig. 1) has two locked loops: a phase-locked loop for phase and frequency synchronization, and a novel amplitude-locked loop for fundamental amplitude determination. The input,

$$x_I(t) = \sum_{k=1}^{\infty} C_k \sin(k\omega_o t + \phi_k) \tag{1}$$

is a periodic waveform with no dc component. The output of the PLL (pre-tuned to a free-running frequency of ω_o) which is purely sinusoidal, is given a 90° phase shift in order to bring it in phase with the fundamental component of the input. Thus,

$$x_P(t) = B_P \sin(\omega_o t + \phi_1). \tag{2}$$

The essential idea is to compare the instantaneous values of the input, x_I and the output, x_O (scaled version of x_P) and to adjust the scaling factor (a_O) by feedback in order to minimize the error. The integrator and the second-order low-pass filter (SOLF) are chosen such that the above operation is performed only on the fundamental component of x_I, thereby desensitizing the loop to all harmonics. Therefore in the steady-state, the output x_O exactly locks on to the fundamental component of x_I (both phase and amplitude) and the signal x_E is the sum of all harmonic components in x_I. In other words, a_O settles to a dc (A_O) such that $A_O B_P$ is the amplitude of the fundamental component of x_I. The integrator gives the additional advantage of zero steady-state error.

In this section, an approximate analysis of the transient operation of the loop and subsequently, an approximate linear time-invariant model for the proposed VLL are presented. The SOLF used here has the standard form as given in (3).

$$H(s) = \frac{1}{\frac{s^2}{\omega_n^2} + \frac{s}{Q\omega_n} + 1} \tag{3}$$

It should be noted here that the SOLF while filtering-out the higher order harmonics, helps in amplifying the residual fundamental by a gain depending on the choice of Q. It also provides 90° phase lag at ω_n which is required for achieving 180° phase lag for optimum negative feedback, as will be explained in the following section.

A. Approximate Transient Analysis

It can be seen that the proposed VLL is a time-varying system since the multiplier may be visualized as an amplifier whose gain varies with time as x_P. An exact and rigorous analysis of such an LTI system would involve the use of complex transforms at the expense of an intuitive feel for its working. Therefore the authors present an approximate analysis which gives a better insight into the working of the loop. Assume, for simplicity, that x_I is a pure sinusoid with frequency ω_o, amplitude $C_1 u(t)$, and $\phi_1 = 0$. Assuming the PLL amplitude B_P as unity, the amplitude of x_O is now $A_O(t)$ the time-varying dc component in a_O. The following analysis is performed for a step change of magnitude C_1, in the input amplitude. The PLL is assumed to have attained steady-state for the purpose of analysis.

At any instant during the transient, the error signal in the loop is,

$$\begin{aligned} x_E(t) &= x_I(t) - A_O(t)x_P(t) \\ &= C_1 \sin(\omega_o t) - A_O(t)\sin(\omega_o t) \\ &= [C_1 - A_O(t)]\sin(\omega_o t). \end{aligned} \tag{4}$$

This error signal is a sinusoid of frequency ω_o which, after passing through the integrator and low-pass filter, undergoes a phase shift of ϕ_o and a gain of $\frac{G}{\omega_o} G_{lp}$, where G_{lp} is the gain of the SOLF at ω_o. Therefore the signal a_O may be expressed as,

$$a_O(t) = \frac{G}{\omega_o} G_{lp}[C_1 - A_O(t)]\sin(\omega_o t + \phi_o). \tag{5}$$

This signal then gets multiplied by x_P to produce a dc component and a $2\omega_o$ component in x_O. Mathematically,

$$x_O(t) = \frac{G_{lp}G}{\omega_o}[C_1 - A_O(t)]\sin(\omega_o t + \phi_o)\sin(\omega_o t). \tag{6}$$

This can be resolved into a dc component and a $2\omega_o$ component as shown in (7).

$$x_O(t) = \frac{G_{lp}G[C_1 - A_O(t)]}{\omega_o}\left[\frac{\cos(\phi_o) - \cos(2\omega_o t + \phi_o)}{2}\right] \tag{7}$$

Since x_O appears in x_E, x_E contains an ω_o component, a dc component as well as a $2\omega_o$ component. The $2\omega_o$ component

is assumed to be sufficiently attenuated by the low-pass filter and hence has little effect on the loop operation. However, the dc component is of prime importance since it is responsible to drive the integrator to the requisite value. After accounting for the inversion of x_O at the subtractor, this dc component is given by,

$$X_E(t) = -\frac{G_{lp}G}{2\omega_o}[C_1 - A_O(t)]\cos(\phi_o). \tag{8}$$

Since this signal directly feeds the integrator, it sets the rate at which the integrator output changes and therefore decides how fast $A_O(t)$ reaches C_1. Notice that, the difference $[C_1 - A_O(t)]$ must result in a dc error component with the same sign, so as to ensure corrective action through negative feedback. From (8), it follows that $\cos(\phi_o)$ must be negative and as large as possible (in magnitude) to achieve dc negative feedback and minimum settling time respectively. The optimal criterion which meets the above requirements is $\cos(\phi_o) = -1$ or $\phi_o = \pm 180^\circ$ which leads to,

$$\phi_o^{opt} = \underbrace{\text{SOLF lag}|_{\omega_o=\omega_n}}_{-90^\circ} + \underbrace{\text{integrator lag}}_{-90^\circ}. \tag{9}$$

For values of ω_o different from ω_n (within certain limits), the loop performs suboptimally. The permissible range of ω_o is discussed in Section V on stability analysis.

B. Approximate LTI model

This section describes the evolution of an approximate *time-invariant* model for the proposed VLL. The effect of variations in the fundamental input amplitude identified by $C_1(t)$ is considered here. The model facilitates the selection of parameters – G and Q. It takes into account only the effect of the dc component produced by the fundamental error signal. The effects of higher frequencies are neglected on the assumption that they are sufficiently attenuated by the SOLF-integrator combination.

At any instant of time, the dc component in x_E is given by (8). When ω_o is sufficiently close to ω_n, $G_{lp} \approx Q$ and $\phi_o \approx -180^\circ$. This implies,

$$X_E(t) = \frac{QG}{2\omega_o}[C_1(t) - A_O(t)]. \tag{10}$$

Taking Laplace transform of (10) we get,

$$X_E(s) = \frac{QG}{2\omega_o}[C_1(s) - A_O(s)]. \tag{11}$$

From Fig. 1, we also get,

$$A_O(s) = \frac{G}{s}H(s)X_E(s). \tag{12}$$

Substituting for $X_E(s)$ from (11) in (12),

$$A_O(s) = \frac{G}{s}\left[\frac{1}{\frac{s^2}{\omega_n^2} + \frac{s}{Q\omega_n} + 1}\right]\frac{QG}{2\omega_o}[C_1(s) - A_O(s)]. \tag{13}$$

On further simplification,

$$\frac{A_O(s)}{C_1(s)} = \frac{1}{\frac{s^3}{G^2Q\omega_o/2} + \frac{s^2}{G^2Q^2/2} + \frac{s}{G^2Q/(2\omega_o)} + 1}. \tag{14}$$

IV. Steady-state analysis

In the steady-state, one may assume that the amplitude of the VLL output closely follows that of the fundamental of the input. In other words, the signal a_O will be predominantly a dc quantity, closely tracking $C_1(t)$. Based on this assumption the following analyses are presented.

A. Analysis for Amplitude Modulated Inputs

When the input amplitude is modulated at sufficiently low frequencies (ω_m), the output amplitude manages to follow closely. It is assumed that a_O contains only the modulating frequency (ω_m) and dc. However, in reality, a_O also contains a ripple of frequency $(\omega_o - \omega_m)$ and $(\omega_o + \omega_m)$, which when multiplied by x_P are, in turn, responsible for the sustenance of the ω_m component in a_O. The linear time-invariant model developed in the previous section *exactly* represents the system for such inputs. A feedback architecture for the same model is presented in Fig. 2 to assist designers in the application of LTI control system techniques for optimizing its tracking abilities. The derivation of Fig. 2 is evident from (13). However, it is to be noted that the original system is time-varying and hence this model cannot be used for conducting stability analysis.

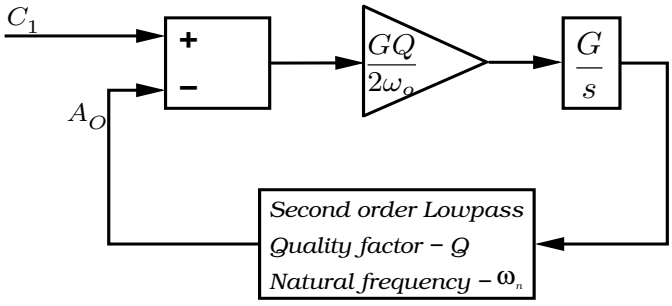

Fig. 2. LTI model of the VLL

B. Ripple factor in the Output Amplitude

Ideally in the steady-state, the signal a_O must be a dc of magnitude C_1. However, in the presence of harmonics, a_O contains the dc and attenuated versions of the harmonics in x_I. Since x_O follows the fundamental in x_I, x_E contains only the sum of all harmonics present in x_I. The harmonics are attenuated by the integrator and the SOLF, leaving a ripple in a_O which may be quantified by,

$$\text{Ripple Factor of } a_O = \frac{G\sqrt{\sum_{k=2}^{\infty}\frac{H^2(k\omega_o)}{(k\omega_o)^2}C_k^2}}{C_1}. \tag{15}$$

V. Stability analysis

The LTI model developed in Section III-B cannot be used to find values of critical G, for a given Q, since it takes into account only the effect of dc caused by the $1\omega_o$ component in the loop. For larger G, the $2\omega_o$ component in (7) cannot be neglected despite attenuation by the SOLF. The surviving $2\omega_o$ component gets multiplied by x_P to produce ω_o and $3\omega_o$ components. This ω_o component appears alongside the original ω_o component (due to the error $C_1(t) - A_O(t)$) thereby giving the effect of an increased dc loop-gain. The exact calculations of these higher order effects can be quite tedious and hence the stability analysis is carried out by conducting experiments with Q as a parameter. The result is plotted as shown Fig. 3 for $\omega_o = \omega_n = 100\pi$ rad/s. The stable and unstable regions are marked and the designer has to keep this in mind while choosing G in relation to Q or vice-versa.

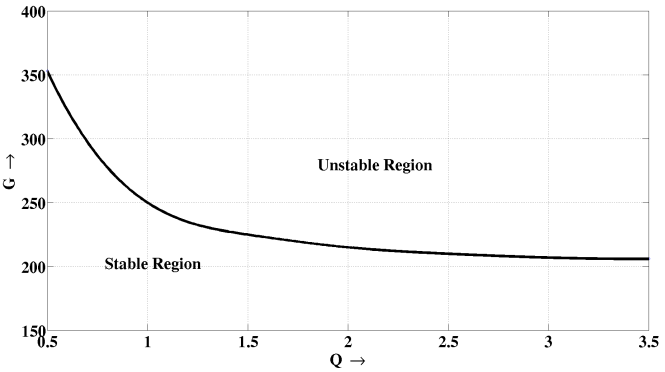

Fig. 3. Limits of stability with Q as a parameter

Further, the system is stable only for a range of ω_o below the nominal value (ω_n). Note that, if ω_o is decreased to such an extent as to make the attenuation of the $2\omega_o$ component in (7) negligible, the effective loop gain increases by the same process as explained earlier. However, this does not apply when ω_o is increased beyond ω_n. In such situations, the $2\omega_o$ component is still attenuated sufficiently in relation to ω_o and hence its effect is neglected. However, higher settling times and suboptimal responses are observed due to the fact that $|\cos(\phi_o)| < 1$ and $G_{lp} < Q$ in (8). Therefore the proposed VLL has a lower limit on ω_o (for given G and Q) due to stability restrictions, whereas the upper limit is dictated by the settling time requirements.

VI. Design considerations

In this section, a few thumb-rules are presented for designing the proposed VLL. The designer may arrive at a more optimized VLL by fine-tuning the system through computer simulations after following these general rules.

A. PLL Design

The PLL performance can be optimized by well established techniques [9]. Note that the proposed VLL output will be of the same frequency as that output by the PLL. Therefore it is necessary to design the PLL with a free-running frequency close to the fundamental frequency component in the input.

B. Choice of G

Note that (14) is applicable to any type of input amplitude function $C_1(t)$. As a special case, to show the effect of amplitude modulation, consider an input modulated by,

$$C_1(t) = C_0 + C_m \sin(\omega_m t), \tag{16}$$

where C_0 is the dc part of C_1 and C_m is the amplitude of the sinusoidal modulation with modulation frequency ω_m. From (14) the output amplitude lags by,

$$\theta = \tan^{-1}\left[\frac{2Q\omega_m}{\omega_o}\left(\frac{\omega_o^2 - \omega_m^2}{G^2Q^2 - 2\omega_m^2}\right)\right]. \tag{17}$$

A properly designed system would be able to closely follow changes in frequency and amplitude of the fundamental input. In other words, the phase lag in amplitude must be as small as possible. Therefore from (17), it follows that the denominator $\omega_o(G^2Q^2 - 2\omega_m^2)$ must be as large as possible. This may be achieved by utilizing a very large gain G. Since θ is small for such a system, we use the approximation that $\tan^{-1}\theta = \theta$. Therefore (17) now becomes,

$$\theta \approx \frac{2Q\omega_m}{\omega_o}\left(\frac{\omega_o^2 - \omega_m^2}{G^2Q^2 - 2\omega_m^2}\right). \tag{18}$$

Further note that $\omega_o \gg \omega_m$. Also, since G is chosen to be large enough to make the denominator of (18) high,

$$\theta \approx \frac{2\omega_o\omega_m}{G^2Q}. \tag{19}$$

Using (19) the sensitivity of θ with respect to G is as follows,

$$\frac{\partial\theta}{\partial G} = \frac{-4\omega_o\omega_m}{Q}\frac{1}{G^3}. \tag{20}$$

From (20), it follows that the sensitivity of the phase lag to variations in G is low when G is large. Therefore in practical systems, it is advisable to include a high gain in the loop for quicker response, small phase lag and to increase the overall robustness of the system.

C. Choice of Q

Using (19), the sensistivity of θ with respect to variations in Q is calculated as follows,

$$\frac{\partial\theta}{\partial Q} = \frac{-2\omega_o\omega_m}{G^2}\frac{1}{Q^2}. \tag{21}$$

From (21) one may conclude that sensitivity of phase lag to variations in Q is low when Q is high and that a high value of G already ensures low sensitivity. However, it is not advisable to have a very large Q since the system becomes highly oscillatory and settling-time increases. Also, a higher Q translates to a lower range of ω_o over which $\phi_o \approx -180^\circ$ (criterion for optimal performance). Therefore the quality factor of the SOLF has a dominant effect on the settling time of the system and also on the dynamic range of input frequency.

VII. Simulation results

Extensive simulation studies were conducted on the proposed VLL using MATLAB® and Simulink®. The system is designed for a specific natural frequency (i.e., 50Hz), and to meet the requirements of, harmonic extraction and tracking amplitude modulation. Hence various features of the system with $\omega_n = 100\pi$ rad/s, $Q = 2$, and $G = 180$ were explored for different inputs. The results are presented in what follows.

A. Response to Step Input

The simulation results of the VLL and the LTI model for a step change of $+0.5$ in the fundamental input amplitude at $t = 0.2$s are shown in Fig. 4 and Fig. 5. The purpose of this test is to estimate the settling time of the system and to compare it with the response from the LTI model. The input for the proposed VLL is,

$$x_I(t) = 0.5[u(t) + u(t - 0.2)]\sin(100\pi t). \tag{22}$$

Hence the input to the LTI model is $C_1(t)$ which is,

$$C_1(t) = 0.5[u(t) + u(t - 0.2)]. \tag{23}$$

It is observed that the output settles to steady-state within 2% error within about three cycles. As observed in Fig. 5, the settling times are matching for the system and its LTI model.

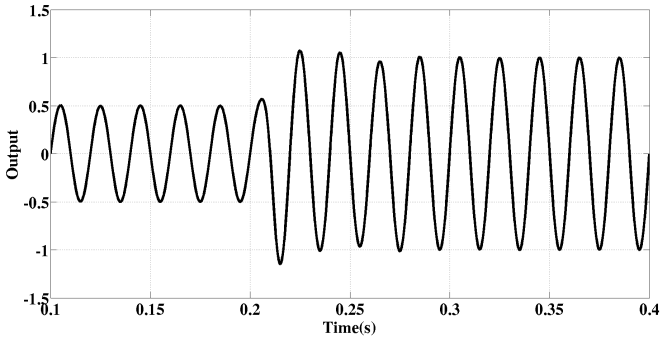

Fig. 4. Simulation result of the actual system to a step change in amplitude

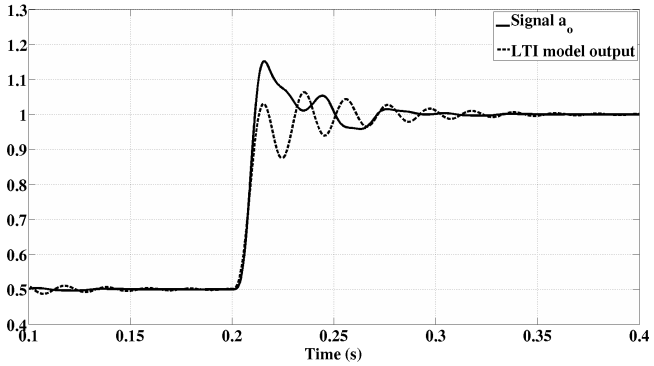

Fig. 5. Comparison of LTI model response and actual system output amplitude to a step change in amplitude

B. Response to Input Amplitude Modulation

The VLL performance was also investigated for an amplitude modulated sine as given in (16) with $C_0 = 1$, $C_m = 0.2$ and $\omega_m = 4\pi$ rad/s. Hence,

$$x_I(t) = [1 + 0.2\sin(4\pi t)]\sin(100\pi t). \tag{24}$$

Fig. 6 displays an area zoomed to around one cycle of the modulating signal in order to clearly show the negligible phase lag in a_O and also the exactness of the LTI model. It is useful to remember that a_O is the instantaneous amplitude of the output, to meaningfully interpret the results. The discrete Fourier series (DFS) of the ripple in a_O revealed the presence of 48 Hz and 52 Hz components as predicted in Section IV-A.

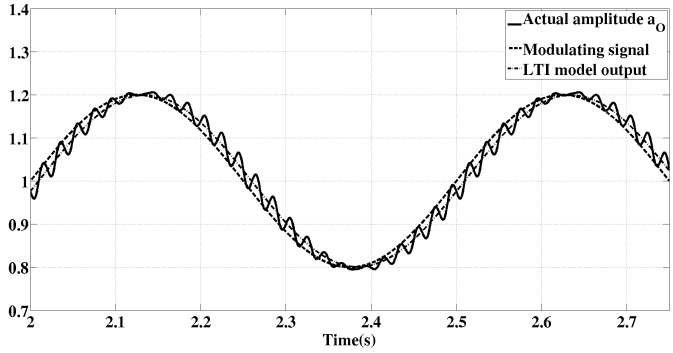

Fig. 6. Comparison of LTI model response and actual system output amplitude to an input whose amplitude is modulated

C. Harmonics Attenuation

Studies on distortion of the output in the presence of harmonics in the input signal are shown in Fig. 7, Fig. 8, and Fig. 9. The applied input is a square wave of unit amplitude and frequency 50 Hz. Fig. 7 and Fig. 8 show the VLL outputs which are the extracted fundamental component and harmonics of the square wave, respectively. A DFS of x_I and x_O are taken and the results are presented in Fig. 9. It can be observed that the amplitude of fundamental components of x_I and x_O are perfectly matched and that the harmonic amplitudes roll off at a rate approximately equal to 360 dB/dec. However, the VLL does introduce a small amount of distortion at the output which is evident by the presence of even harmonic components in the DFS plot, despite their absence in the input.

D. Noise Rejection

Simulation studies on the noise rejection capabilities of the VLL were conducted. Fig. 10 shows the input, which is a sine wave of 100π rad/s with band-limited white noise, and the corresponding output. For an input signal-to-noise-and-distortion ratio (SNDR) of 7 dB, the output SNDR was observed to be 26.3 dB.

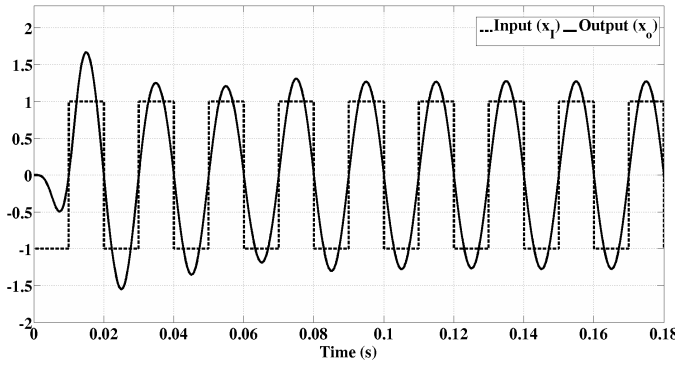

Fig. 7. Output for square wave input

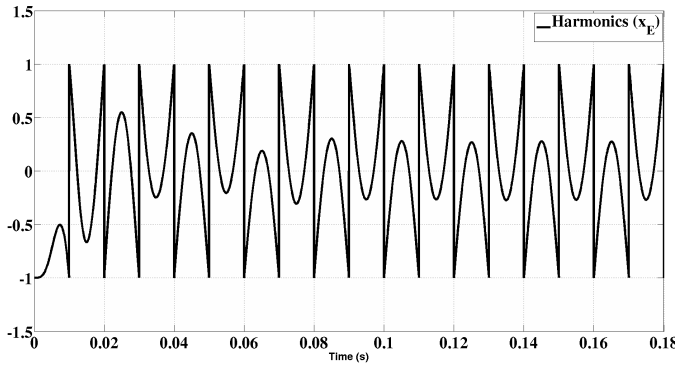

Fig. 8. Harmonic output for square wave input

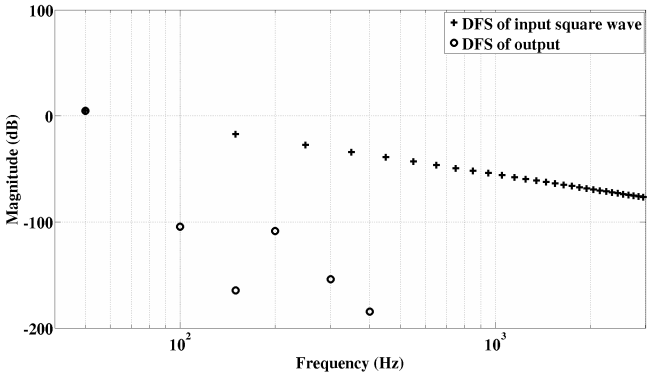

Fig. 9. Frequency spectrum analysis for a square wave input

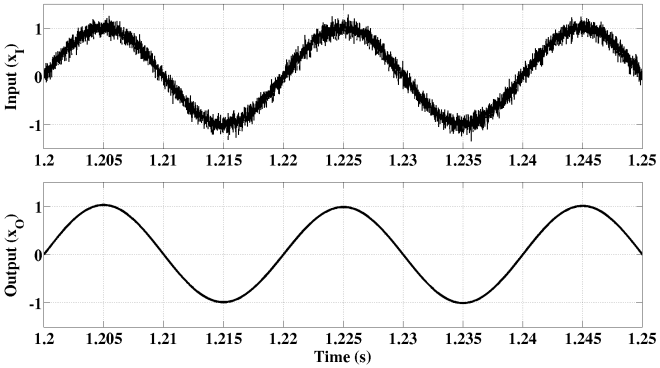

Fig. 10. Performance under noisy conditions

VIII. Conclusions

A novel scheme for obtaining synchronized selective-frequency amplitude-locking on distorted signals is presented. An intuitive explanation of the working of the loop is presented. A comprehensive LTI model for the system is developed to facilitate the design process. It is found that the model truly represents the actual system as far as the settling time, steady-state response, and modulation properties are concerned. However the stability behaviour is not captured in the LTI model for the obvious reason that the actual scheme is time-variant. Hence stability margin is determined by means of experiment. Clear explanations are given for the selection of G and Q. Performance claims are supported by simulation results. The features of the proposed scheme are as follows:

- it has features similar to a PLL.
- the performance can be optimized by appropriate choice of G and Q.
- the transient response is better (about three cycles), has excellent insensitivity to harmonics, and noise rejection.
- the amplitude tracking is determined by the product of depth of modulation and the frequency of modulation.
- the scheme is a time-variant system.

It can find applications in:

- synchronous separation of the fundamental and harmonics in a distorted periodic waveform.
- amplitude and frequency tracking
- noise rejection.
- amplitude demodulation/peak detection.

Hardware implementation of the proposed scheme for Active Filtering of harmonics in power systems is underway.

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